REMARKS

Claims 1 to 49 were pending in the Application at the time of examination. The Examiner provisionally rejected Claims 1 to 49 as claiming the same invention as claims 1 to 26 of co-pending application no. 09/982,459. The Examiner provisionally rejected Claims 1 to 49 under the judicially created doctrine of obviousness-type double patenting over Claims 1 to 77 of co-pending Application no. 09/982,452. The Examiner rejected Claims 1 to 49 under 35 U.S.C. 103(a) as obvious over the Camporese et al. reference (US 6,205,571) in view of the Graef reference (US 6,305,001).

Applicants have cancelled Claims 29 and 30, without prejudice. Applicants have amended Claims 27 and 33. Consequently, Claims 1 to 28 and 31 to 49 remain in the Application.

PROVISIONAL REJECTION OF CLAIMS 1 TO 49 BASED ON APPLICATION 09/982,459

The Examiner provisionally rejected Claims 1 to 49 as claiming the same invention as claims 1 to 26 of co-pending application no. 09/982,459.

Applicants note that Application no. 09/982,459 is now abandoned. Consequently, Applicants respectfully submit that the provisional rejection of Claims 1 to 49 as claiming the same invention as claims 1 to 26 of co-pending application no. 09/982,459 is now moot.

PROVISIONAL REJECTION OF CLAIMS 1 TO 49 BASED ON APPLICATION 09/982,452

The Examiner provisionally rejected Claims 1 to 49 under the judicially created doctrine of obviousness-type double

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> **simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;**
> **combining the plurality of simulations to form the complete clock net;**
> storing the plurality of simulation results in a Clock Data Model; and
> evaluating the plurality of simulation results to determine whether the results converge.

As shown above, Applicants' Claims 1, 14 and 37 specifically recite:

> **simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;**
> **simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;**
> **combining the plurality of simulations to form the complete clock net;**

or words to the same effect.

The Examiner has cited Column 12, lines 12 to 23 and Column 11, lines 33 to 50 of the Camporese et al reference as teaching the above limitations. Column 11, line 33 to column 12, line 25 of the Camporese et al reference reads as follows:

> As referenced in FIG. 7, step 740, it is thus advisable to perform a final full-accuracy extraction and simulation of the actual tuned network with these approximations removed. This is accomplished by implementing the optimum wiring and device sizes in a design with the fill uncut X-Y grid wiring in place (e.g., as graphically depicted in FIG. 11), preferably including all twig wires and pin loads (FIG. 5), extracting this design to create a full electrical net list, and performing an accurate transient simulation with a high accuracy nonlinear circuit simulation method such as SPICE, to evaluate

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the skew, power, and signal integrity of the tuned clock network with maximum accuracy. This final extraction and simulation may take significant time, but since it can be performed at the same time as other final checking processes, in practice the final extraction and full simulation of the clock distribution network does not add to the total chip design time.

As VLSI chip designs evolves, the clock loads, the twig wiring, and minor blockage avoidance modifications may change a number of times. In some cases, once the desired modifications have been made, either an approximate or final extraction and full simulation clock distribution network may show that re-tuning of the clock distribution is needed, (see FIG. 7, step [745]). If re-tuning is required, the process can be repeated by returning to step 715. This re-tuning can be facilitated if a clock distribution contract or abstract exists describing the maximum wire tracks and device area that may result from the tuning process. This contract then results in upper bounds on tunable parameters such wire sizes and spaces, or buffer sizes, and these limits result in boundary conditions for the nonlinear optimization program. To further reduce power and wiring used by the clock distribution network, the electrical current in each segment of the X-Y grid can be determined from the transient simulation of the full electrical net list. A method can be used to identify X-Y grid wire segments with small currents, which are thus relatively unnecessary, and a fraction of these unnecessary grid segments can be deleted, especially if there are no twig wires using such a grid wire segment, or the twig wiring can be easily modified to use another X-Y grid segment. This grid deletion step can then be treated like other design modifications described above such as blockage avoidance or clock pin load changes: grid segment deletions may require modification of the local twig wiring, final checking, and if warranted, re-tuning. Portions of some tree wiring levels may also be removed by a similar tree branch deletion method. In fact it may be obvious, for example, that one or more comers of the chip may contain no clock pins, or only pins with much greater tolerance for clock skew, in which case the low skew network trees and grid wires in that region could be deleted. These modifications should be reflected in the smoothing function boundary

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conditions or smoothing coefficients so that the smoothing function still accurately simulates the effect of the modified X-Y grid wires.

A clock distribution network and tuning method combining the characteristics of tunable wiring trees and an X-Y grid has been disclosed that significantly reduces skew in large high-speed VLSI circuits, while also reducing design time.

Applicants respectfully submit that the Examiner has failed to show where in the section of the Camporese et al reference shown above, where in any portion of the Camporese et al reference, where in any portion of the Graef reference, or where in any combination of the Camporese et al reference and the Graef reference, it is disclosed, taught or suggested:

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net;

as recited in Applicants Claims 1, 14, and 37. Consequently, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 14, and 37 and allow Claims 1, 14 and 37 to issue.

Claims 2 to 13 depend, directly or indirectly, on Claim 1. Consequently, Claims 2 to 13 include all of the features and limitations of Claim 1 and are therefore patentable over the Camporese et al. reference, the Graef reference, or any combination of the Camporese et al. reference and the Graef reference for at least the reasons discussed above.

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Consequently, Applicants respectfully request allowance of Claims 2 to 13.

Claims 15 to 26 depend, directly or indirectly, on Claim 14. Consequently, Claims 15 to 26 include all of the features and limitations of Claim 14 and are therefore patentable over the Camporese et al. reference, the Graef reference, or any combination of the Camporese et al. reference and the Graef reference for at least the reasons discussed above. Consequently, Applicants respectfully request allowance of Claims 15 to 26.

Claims 38 to 49 depend, directly or indirectly, on Claim 37. Consequently, Claims 38 to 49 include all of the features and limitations of Claim 37 and are therefore patentable over the Camporese et al. reference, the Graef reference, or any combination of the Camporese et al. reference and the Graef reference for at least the reasons discussed above. Consequently, Applicants respectfully request allowance of Claims 38 to 49.

Applicants have amended Claim 27. Applicants' independent Claim 27, as amended, recites, with emphasis added:

> An apparatus for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the apparatus comprising:
>
> a partitioner for horizontally and vertically partitioning the complete clock net into a global clock net and a plurality of local clock nets, **wherein;**
>
> **the partitioner vertically sub-partitions at least one of the plurality of local clock nets down into at least one sub-local clock net;**
>
> at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, **wherein;**
>
> **the at least one local clock net simulator simulates the at least one sub-local clock net prior to simulating the corresponding local clock net;**

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> a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;
> a merging unit for combining the plurality of simulations to form the complete clock net;
> a Clock Data Model for storing the plurality of simulation results; and
> a convergence evaluator for evaluating the plurality of simulation results to determine whether the results converge.

Applicants respectfully submit that the Examiner has failed to show where in the Camporese et al reference, where in the Graef reference, or where in any combination of the Camporese et al reference and the Graef reference, it is disclosed, taught or suggested:

> a partitioner for horizontally and vertically partitioning the complete clock net into a global clock net and a plurality of local clock nets, **wherein;**
> **the partitioner vertically sub-partitions at least one of the plurality of local clock nets down into at least one sub-local clock net;**
> at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, **wherein;**
> **the at least one local clock net simulator simulates the at least one sub-local clock net prior to simulating the corresponding local clock net;**

as recited in Applicants' Claim 27, as amended. Consequently, Applicants respectfully request the Examiner withdraw the rejection of Claim 27, as amended, and allow Claim 27 to issue.

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Claims 28 to 36 depend, directly or indirectly, on Claim 27. Consequently, Claims 28 to 36 include all of the features and limitations of Claim 27, as amended, and are therefore patentable over the Camporese et al. reference, the Graef reference, or any combination of the Camporese et al. reference and the Graef reference for at least the reasons discussed above. Consequently, Applicants respectfully request allowance of Claims 28 to 36.

CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 11, 2005.

Attorney for Applicant(s) — August 11, 2005 Date of Signature

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